REMARKS

Applicant respectfully requests consideration of the subject application as amended herein. This Amendment is submitted in response to the Office Action mailed on 4/20/2009. Claims 1, 2, 4-10, 12, and 14-23 are rejected. In this Amendment, claims 1, 6, and 12 have been amended. No new matter has been added. No claims have been canceled. Therefore, claims 1, 2, 4-10, 12, and 14-23 are presented for examination.

Priority

The Office Action denied Applicants' claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. Applicant declines to challenge the denial of the priority claim at this time, but reserves the right to challenge the denial of the priority claim at a later date.

Rejections Under 35 U.S.C. §103

Claims 1, 2, 4-10, 12, 14-20, and 23

The Office Action has rejected claims 1, 2, 4-10, 12, and 14-23 under 35 U.S.C § 103 as being allegedly obvious over U.S. Patent No. 5,371,878 to Coker (hereinafter "Coker"), in view of "How Debuggers Work", by Jonathan B. Rosenberg (hereinafter "Rosenberg"), and further in view of U.S. Patent No. 5,968,135 to Teramoto, et al., (hereinafter "Teramoto").

Claim 1, as amended, recites:

1.   A boot method for synchronizing a microcontroller and a virtual microcontroller of an In-Circuit Emulation system in lock-step, comprising:
        in the microcontroller, executing a set of boot code to carry out initialization;

in the virtual microcontroller, executing a set of timing code to enable a lock-step synchronization with the microcontroller, wherein the set of timing code is a dummy code timed to take the same number of clock cycles as the microcontroller uses to execute the set of boot code, wherein the set of timing code is functionally different from the set of boot code, and wherein the set of boot code is stored within the microcontroller and the set of boot code is inaccessible to the virtual microcontroller;

simultaneously halting both the microcontroller and the virtual microcontroller; and

restarting the microcontroller and the virtual microcontroller to execute instructions in lock-stepped synchronization. (Emphasis added.)

Claim 10 recites:

simultaneously halting both the microcontroller and the virtual microcontroller by branching to the assembly instruction line 0;

Claim 12, as amended, recites:

simultaneously halting both the tested device and the virtual processor;

Coker describes a system that shadows execution of an embedded computer system (Abstract). The Office Action admits that Coker does not teach or suggest simultaneously halting both a microcontroller and a virtual microcontroller, as recited in amended claim 1 and claim 10, nor does Coker teach or suggest simultaneously halting both a tested device and a virtual processor, as recited in amended claim 12.

In contrast with claim 1, as amended, Rosenberg does not disclose, at the section cited in the Office Action, that any of the processors is a virtual microcontroller, much less describe simultaneously halting both a

microcontroller and a virtual microcontroller, as is recited in amended claims 1 and 10. Rosenberg therefore does not teach or suggest this feature of amended claims 1 and 10. Rosenberg also does not teach or suggest simultaneously halting both a tested device and a virtual processor, as recited in amended claim 12.

The Office Action does not allege that Teramoto teaches or suggests simultaneously halting both a microcontroller and a virtual microcontroller. Furthermore, Teramoto does not, at the section cited in the Office Action, mention using a virtual microcontroller and therefore does not teach or suggest simultaneously halting both a microcontroller and a virtual microcontroller, as recited in amended claims 1 and 10. Teramoto also does not teach or suggest simultaneously halting both a tested device and a virtual processor, as recited in amended claim 12.

Because none of Coker, Rosenberg, or Teramoto teaches or suggests simultaneously halting both a microcontroller and a virtual microcontroller, the combination of Coker, Rosenberg, and Teramoto cannot be properly interpreted as disclosing the claimed element. Claims 1 and 10 are therefore not rendered obvious by the combination. Because none of Coker, Rosenberg, or Teramoto teaches or suggests simultaneously halting both a tested device and a virtual processor, the combination of Coker, Rosenberg, and Teramoto cannot be properly interpreted as disclosing the claimed element. Independent claim 12 is therefore not rendered obvious by the combination. Dependent claims 2, 4-9, 14-20, and 23 depend from one of independent claims 1, 10, or 12, and are also not rendered obvious by the combination. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 1, 2, 4-10, 12, 14-20, and 23 over Coker, Rosenberg, and Teramoto, under 35 U.S.C § 103.

Claim 21

The Office Action has rejected claim 21 as being allegedly obvious over
Coker in view of Rosenberg, further in view of Teramoto, and further in view of
"Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation
System" by Matthew Dahl, Jonathan Babb, Russel Tessir, Silvina Hanono, David
Hoki, and Anant Agarwal (hereinafter "Dahl") and further in view of "A
Reconfigurable Logic Machine for Fast Event-Driven Simulation" by Jerry Bauer,
Michael Bershteyn, Ian Kaplan, and Paul Vyedin (hereinafter "Bauer").

Claim 21 depends from claim 12. As previously discussed, none of Coker,
Rosenberg, or Teramoto teaches or suggests the feature of claim 12 of
simultaneously halting a microcontroller and a virtual microcontroller.

Dahl describes emulation of a microprocessor using an FPGA (Abstract).
Bauer describes increasing simulation speed by using hardware emulation
(Introduction, Paragraph 2). Neither Dahl nor Bauer teaches or suggests a
process of halting microcontrollers at the sections cited in the Office Action,
much less simultaneously halting a microcontroller and a virtual microcontroller.

Therefore, since none of Coker, Rosenberg, Teramoto, Dahl, or Bauer
teaches or suggests simultaneously halting a microprocessor and a virtual
microprocessor, the combination of Coker, Rosenberg, Teramoto, Dahl, and
Bauer cannot be properly interpreted as disclosing the claimed feature as recited
in claim 12. Claim 21, which depends from claim 12, is therefore not rendered
obvious by the combination. Accordingly, Applicant respectfully requests
withdrawal of the rejection of claim 21 over the combination under 35 U.S.C §
103.

Claim 22

The Office Action has rejected claim 22 as being allegedly obvious over Coker in view of Rosenberg, further in view of Teramoto, and further in view of U.S. Patent No. 4,575,534 to Matyas et al. (hereinafter "Matyas").

Claim 22 depends from claim 1. As previously discussed, none of Coker, Rosenberg, or Teramoto teaches or suggests the feature of claim 1 of simultaneously halting a microcontroller and a virtual microcontroller.

Matyas describes a cryptographic method for allowing an encrypted program to be run only on particular computers (Abstract). Matyas also describes code containing serial numbers, passwords, and algorithms (Column 13, lines 1-21). However, Matyas does not teach or suggest using a virtual microcontroller, much less simultaneously halting both a microcontroller and a virtual microcontroller. Matyas therefore does not teach or suggest this feature of claim 1.

Because none of Coker, Rosenberg, Teramoto, or Matyas teaches or suggests simultaneously halting a microcontroller and a virtual microcontroller, the combination of Coker, Rosenberg, Teramoto, and Matyas cannot be properly interpreted as disclosing the claimed feature of claim 1, as amended. Claim 22, which depends from claim 1, is therefore not rendered obvious by the combination. Accordingly, Applicant respectfully requests withdrawal of the rejection of claim 22 over Coker, Rosenberg, Teramoto, and Matyas under 35 U.S.C § 103.

Conclusion

Claims 1, 2, 4-10, 12, and 14-23 are currently pending. In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

Should the Examiner have any questions regarding this response or the application in general, the Examiner is urged to contact the Applicant's attorney, Kerry Liang, by telephone at (408) 545-7399. All correspondence should continue to be directed to the address given below.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Respectfully Submitted,

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